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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,581	07/22/2003	Isamu Kobori	07977-024003	6534

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EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	
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09/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/623,581	KOBORI ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-36 and 46-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-36 and 46-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/623,506.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/03/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment and RCE filed on 4/30/07 and 7/03/07, respectively. Currently, claims 16-36 and 46-60 are pending.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 7/03/07 has been entered.

Information Disclosure Statement

2. The information disclosure statement was (IDS) submitted on 7/03/07. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

3.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 16-36 and 46-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., US Patent 6,198,133 in view of Nakamura et al., Japanese Patent Application JP6-123896.

Yamazaki discloses the semiconductor method substantially as claimed. See figures 1-11D, and corresponding text where, Yamazaki shows, pertaining to claims 16, 22 and 28, a method for forming an active matrix circuit comprising a transistor, said method comprising: doping a p-type impurity **619-620** into a semiconductor layer **603-605** by ion doping to form a p-type impurity region in said semiconductor layer, said semiconductor layer comprising a part to become a channel region adjacent to said p-type impurity region (figure 6E; col.7, lines 64-67; col. 8, lines 1-5); forming a gate electrode **609/611** adjacent to said part to become said channel region (figure 6A; col. 7, lines 20-23); activating said p-type impurity by annealing (figure 6E; col. 8, lines 17-21); and forming an interlayer insulating film **622** comprising a silicon nitride layer and a silicon oxide layer over said semiconductor layer by plasma CVD, said silicon nitride layer and said silicon oxide layer formed over said gate electrode and said semiconductor layer (figure 6F; col. 8, lines 23-27); and forming a conductive multi-layer film, comprising a titanium layer and an aluminum layer over said interlayer insulating film, wherein said transistor of said

active matrix circuit comprise said channel region and said gate electrode and said p-type impurity region (figure 6G; col. 8, lines 28-31). In addition, Yamazaki shows, pertaining to claims 17, 23 and 31, wherein said active matrix circuit is incorporated into a liquid-crystal device (col. 1, lines 12-20 conventional devices). Also, Yamazaki shows, pertaining to claims 18, 24 and 32, wherein said active matrix circuit is incorporated into an image sensor (col. 1, lines 62-67; col. 2, lines 1-7 conventional devices that include image sensors). Yamazaki shows, pertaining to claims 19, 25 and 33, wherein said active matrix circuit is incorporated into a liquid crystal electro-optical device (col. 1, lines 12-20 conventional devices). In addition, Yamazaki shows, pertaining to claims 21, 27 and 35, further comprising crystallizing said amorphous semiconductor island (figure 6A; col. 6, lines 50-67; col. 7, lines 1-5). Also, Yamazaki shows, pertaining to claim 29, wherein said conductive layer comprises an electrode (figure 6A; 7, lines 20-24). Yamazaki shows, pertaining to claim 30, wherein said conductive layer comprises a wiring (figure 6G; col. 8, lines 27-37). In addition, Yamazaki shows, pertaining to claim 36, wherein said conductive layer comprises a multi-layer film including a titanium layer and an aluminum layer (figure 6G; col. 8, lines 27-31).

Yamazaki shows, pertaining to claims 46, 51 and 56, a method for forming an active matrix circuit comprising a transistor, said method comprising: doping a p-type impurity **619-620** into a semiconductor layer by ion doping to form a source region and a drain region in said semiconductor layer, said semiconductor layer **603-605** comprising a part to become a channel region between said source region and said drain region (figure 6E; col.7, lines 64-67; col. 8, lines 1-5); forming a gate electrode **609-611** adjacent to said part to become said channel region (figure 6A; col. 7, lines 20-23); activating said p-type impurity by annealing (col. 8, lines 17-21);

forming a first interlayer insulating film comprising a silicon nitride layer and a silicon oxide layer over said semiconductor layer by plasma CVD, said silicon nitride layer and said silicon oxide layer formed over said gate electrode and said semiconductor layer (figure 6F; col. 8, lines 23-27); forming a conductive layer comprising a titanium and an aluminum over said first interlayer insulating film (figure 6G; col. 8, lines 28-31); forming a second insulating film comprising silicon oxide **632** over said conductive layer (figure 6G; col. 8, lines 31-33); and forming a pixel electrode **633** over said second insulating film, wherein said transistor of said active matrix circuit comprises said channel region and said gate electrode and said source region and said drain region (figure 6G; col. 8, lines 33-36). In addition, Yamazaki shows, pertaining to claims 47, 52, and 57, wherein said active matrix circuit is incorporated into a liquid crystal display (col. 1, lines 12-20 conventional devices). Also, Yamazaki shows, pertaining to claims 48, 53 and 58, wherein said active matrix circuit is incorporated into an image sensor (col. 1, lines 62-67; col. 2, lines 1-7 conventional devices that include image sensors). Finally, Yamazaki shows, pertaining to claims 50, 55 and 60, further comprising crystallizing said amorphous semiconductor island (figure 6A; col. 6, lines 50-67; col. 7, lines 1-5).

However, Yamazaki fails to show, pertaining to claims 16, 22, 28, 46, 51 and 56, forming an active layer comprising a plurality of semiconductor islands arranged in parallel to each other over a substrate. In addition, Yamazaki fails to show, pertaining to claims 20, 26, 34, 49 and 54, a method, wherein said semiconductor layer comprises an amorphous semiconductor island having a plane area of 1000 μm^2 or less.

Yamazaki teaches, a plurality of thin film transistors used in the formation of an active matrix circuit device (figures 6G; col. 8, lines 35-41).

Nakamura teaches, connecting in parallel a plurality of thin film transistors and each channel width of the thin film transistors are connected in parallel (drawings 1 and 3; [0009] and [0012]).

It would have been obvious to one of ordinary skill in the art to substitute, forming an active layer comprising a plurality of semiconductor islands arranged in parallel to each other over a substrate, in the method of Yamazaki, pertaining to claims 16, 22, 28, 46, 51 and 56, according to the teachings of Nakamura, with the motivation that, by connecting both a plurality of thin film transistors and each of the narrow channels in parallel, as taught by Nakamura, the hydrogen treatment process can be performed without variation, allowing for a more efficient semiconductor process.

It would have been obvious to one of ordinary skill in the art to incorporate, the method wherein said semiconductor layer comprises an amorphous semiconductor island having a plane area of 1000 μm^2 or less, pertaining to claims 20, 26, 34, 49 and 54, in the method of Yamazaki, according to the teachings of Yamazaki in view of Nakamura, with the motivation that, the conventional active matrix circuits, generally include a plurality of thin film transistor devices used as a driving circuit, where these transistors are formed on semiconductor islands. Therefore, forming an amorphous semiconductor island having an area of 1000 μm^2 or less, are parameters of optimization, where one of ordinary skill in the art would be capable of forming a desired area of the amorphous semiconductor island during routine experimentation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stanetta Isaac
Patent Examiner
August 31, 2007

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER